AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claims 1-2 (Canceled)

Claim 3 (Currently amended): ~~The receiver according to claim 1,~~

A receiver comprising:

a reception front-end for receiving a plurality of pulse signals including at least a first pulse signal and a second pulse signal as a reception signal, wherein a pulse sequence generating time of the second pulse signal is longer than a pulse sequence generating time of the first pulse signal;

a delay circuit for generating a delay signal by delaying a reception front-end output signal output from the reception front-end; and

a delay pulse composition circuit for combining the delay signal with the reception front-end output signal,

wherein a delay time given to the reception front-end output signal by the delay circuit is longer than the pulse sequence generating time of the first pulse signal, and is shorter than the pulse sequence generating time of the second pulse signal;

wherein the reception front end comprises a first antenna which receives both of the first pulse signal and the second pulse signal and a second antenna which receives only the second pulse signal;

wherein the second antenna is narrower in a reception frequency band than the first antenna;

wherein a reception signal received at the first antenna is output to the delay pulse composition circuit, and a reception signal received at the second antenna is output to the delay circuit; and

wherein the delay pulse composition circuit combines the delay signal output from the delay circuit with the reception front-end output signal output from the first antenna.

Claims 4-11 (Canceled)

Claim 12 (Previously presented): A transmitter comprising:

a control signal generating circuit for outputting a control signal which generates a plurality of pulse signals having pulse sequence generating times different from each other;

a pulse generating circuit for generating the plurality of pulse signals by using the control signal; and

a communication state determining circuit for determining a communication state, wherein the transmitter changes the pulse sequence generating time of the pulse signal based on information about communication state determined by the determining circuit.

Claim 13 (Previously presented): The transmitter according to claim 12, wherein an oscillating circuit is used as the pulse generating circuit.

Claim 14 (Previously presented): The transmitter according to claim 13, wherein the oscillating circuit is frequency variable.

Claim 15 (Previously presented): The transmitter according to claim 13, wherein the oscillating circuit works intermittently by using the control signal.

Claim 16 (Previously presented): The transmitter according to claim 12, wherein the transmitter generates at least two signals having different pulse sequence generating times as the plurality of pulse signals.

Claim 17 (Canceled)

Claim 18 (Previously presented): The transmitter according to claim 12, wherein the transmitter changes the pulse sequence generating time of the pulse signal to be shorter based on information about communication state determined good by the determining circuit.

Claim 19 (Previously presented): The transmitter according to claim 12, wherein the transmitter changes the pulse sequence generating time of the pulse signal to be longer based on information about communication state determined poor by the determining circuit.

Claim 20 (Previously presented): The transmitter according to claim 12, wherein a shorter pulse signal is used out of the pulse signals having different pulse sequence generating times from each other for communication between wireless devices of which communication

state is good, and a longer pulse signal is used out of the pulse signals having different pulse sequence generating times from each other for communication between wireless devices of which communication state is poor.

Claim 21 (Previously presented): The transmitter according to claim 12, further comprising an interference detecting circuit for detecting interference with other wireless devices, wherein the pulse sequence generating time of the pulse signal is changed based on interference information detected by the detecting circuit.

Claim 22 (Previously presented): The transmitter according to claim 21, wherein the pulse sequence generating time of the pulse signal is changed to be longer based on information about existing interference detected by the detecting circuit.

Claim 23 (Previously presented): The transmitter according to claim 21, wherein the pulse sequence generating time of the pulse signal is changed to be shorter based on information about no interference detected by the detecting circuit.

Claims 24-29 (Canceled)

Claim 30 (Previously presented): A wireless system comprising a transmitter and a receiver for receiving a signal supplied from the transmitter,

wherein the transmitter includes:

a control signal generating circuit for outputting a control signal which generates a plurality of pulse signals having pulse sequence generating times different from each other;

a pulse generating circuit for generating the plurality of pulse signals by using the control signal; and

a communication state determining circuit for determining a communication state, wherein the transmitter changes the pulse sequence generating time of the pulse signal based on information about communication state determined by the determining circuit; and

wherein the receiver includes:

a reception front end for receiving a plurality of pulse signals including at least a first pulse signal and a second pulse signal as a reception signal, wherein a pulse sequence generating time of the second pulse signal is longer than a pulse sequence generating time of the first pulse signal;

a delay circuit for generating a delay signal by delaying a reception front-end output signal output from the reception front end; and

a delay pulse composition circuit for combining the delay signal with the reception front-end output signal;

wherein a delay time given to the reception front-end output signal by the delay circuit is longer than the pulse sequence generating time of the first pulse signal and is shorter than the pulse sequence generating time of the first pulse signal.